METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

Technical Field

The present invention concerns methods of semiconductor device or integrated circuit manufacturing, particularly methods of forming interconnects from copper and other metals.

Background of the Invention

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then wired, or interconnected, together with aluminum wires to define a specific electric circuit, such as a computer memory. The aluminum wires are typically about one micron thick, or about 100 times thinner than a human hair.

To form the aluminum wires, fabricators sometimes use a dual-damascene metallization technique, which takes its name from the ancient Damascan metalworking art of inlaying metal in grooves or channels to form ornamental patterns. The dual-damascene technique entails covering the components on a wafer with an insulative layer of silicon dioxide, etching small holes in the insulative layer to expose portions of the components underneath, and subsequently etching shallow trenches from hole to hole to define a wiring pattern.

Etching the trenches and holes entails forming a mask, using photolithographic techniques, on the insulative layer. The masks, which typically consists of a material called photoresist, shields some portions of the insulative layer from the etchant and allows the etchant to dissolve away other portions. After etching, fabricators remove the mask to expose the patterned insulative layer. They then blanket the entire insulative layer with a thin sheet of aluminum and polish off

the excess, leaving behind aluminum vias, or contact plugs, in the holes and thin aluminum wires in the trenches.

The complexity of some integrated circuits demand several interconnected levels of wiring. Some circuits, such as microprocessors, have five or six interconnected levels, with each level formed by repeating the basic dual-damascene produce. For example, to form a second wiring level, fabricators apply a new insulative layer over the first wiring layer, form another mask on the new layer, etch holes and trenches into the new layer, remove the mask, blanket the new layer with aluminum, before finally polishing off the excess to complete it.

In recent years, researchers have begun using copper instead of aluminum to form integrated-circuit wiring, because copper offers lower electrical resistance and better reliability at smaller dimensions. Fabrication of copper-wired integrated circuits sometimes follows an extension of the dual-damascene method which includes an additional step of lining the holes and trenches of an insulative layer with a copper-diffusion barrier before blanketing the layer with copper and polishing off the excess. (The diffusion barrier is generally necessary because copper atoms readily diffuse through common insulators, such as silicon dioxide, resulting in unreliable or inoperative integrated circuits.) Typically, the copper-diffusion barrier is more than 30 nanometers thick and consists of tantalum, tantalum nitride, tantalum-silicon-nitride, titanium nitride, or tungsten nitride. Filling the barrier-lined holes and trenches with copper generally entails depositing a thin copper seed layer on the copper-diffusion barrier, electroplating copper on the seed layer, and then polishing off the excess.

The present inventors identified at least two problems with using the extended dual-damascene technique for making the copper wiring. The first is that typical copper-diffusion barriers add appreciable resistance to the copper wiring, and thus negate some promised performance advantages. And, the second is that the number of separate procedures or steps necessary to make the copper wiring using the extended technique makes fabrication both costly and time consuming.

Accordingly, there is a need for better ways of making copper wiring for integrated circuits.

Summary of the Invention

To address these and other needs, the inventors devised unique methods of forming wiring from copper and other desirable metals, some of which allow fabrication of copper wiring with fewer steps and lower electrical resistance than some conventional methods. One exemplary method forms a first mask layer with openings that expose underlying transistor contact regions and then forms on the first mask layer a first metal structure of for example, copper, silver, or gold-based metals, which contacts the transistor contact regions. Next, with the first mask layer still in place, the exemplary method forms a second mask layer with openings that expose portions of the underlying first metal structure and then forms on the second mask structure a second metal structure which contacts exposed portions of the first metal structure.

After formation of these mask layers and metal structures, the exemplary method removes both mask layers in a single removal procedure, leaving a space around and between the metal structures. The first and second metal structures are then coated in a single procedure with a 6-10-nanometer-thick diffusion barrier, such as WSi_xN_y (tungsten-silicon-nitrogen.) And subsequently, the space is filled, in another single procedure, with one or more insulative materials, such as silicon dioxide, an aerogel, or an xerogel.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of an exemplary integrated-circuit assembly 100, including two transistors 214a and 214b and a mask layer 216 with via holes 216a and 216b, and a trench 216c;

Figure 2 is a cross-sectional view of the Figure 1 assembly after formation of conductive structure 218 within holes 216a and 216b and trench 216c;

Figure 3 is a cross-sectional view of the Figure 2 integrated-circuit assembly after formation of a mask layer 220 on conductive structure 218;

Figure 4 is a cross-sectional view of the Figure 3 assembly after formation of a conductive structure 222 on mask layer 220;

Figure 5 is a cross-sectional view of the Figure 4 assembly after removal of mask layers 116 and 220 to define space 224;

Figure 6 is a cross-sectional view of the Figure 5 assembly after forming a diffusion-barrier 226 on conductive structures 218 and 222;

Figure 7 is a cross-sectional view of the Figure 6 assembly after filling space 224 with one or more insulative materials to form a two-level insulative structure 228;

Figure 8 is a block diagram of an exemplary integrated memory circuit which incorporates the present invention.

Description of the Preferred Embodiments

The following detailed description, which references and incorporates Figures 1-8, describes and illustrates specific embodiments of the invention. These embodiments, offered not to limit but only to exemplify and teach the concepts of the invention, are shown and described in sufficient detail to enable those skilled in the art to implement or practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

Figures 1-7 show a number of cross-sectional views of a partial integrated-circuits assembly 100, which taken collectively and sequentially, illustrate a unique exemplary method of making integrated circuits, and more particularly making integrated-circuit wiring in accord with teachings of the present invention. The method, as shown in Figure 1, begins with a known integrated-circuit assembly or structure 100, which can exist within any integrated circuit, a dynamic-random-access memory, for example. Assembly 100 includes a substrate 212. The term "substrate," as used herein, encompasses a semiconductor wafer as well as structures having one or more insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures.

Substrate 212 supports a number of integrated elements 214, for example transistors 214a and 214b. Transistors 214a and 214b are covered by a mask layer 216, which, for example, comprises photoresist. In the exemplary embodiment, the transistors are metal-oxide-semiconductor field-effect transistors (MOSFETs); however, in other embodiments, the transistors are other types of field-effect transistors or bipolar junction transistors, or mixed transistor types. Still other embodiments use other types of integrated devices.

Layer 216 includes two exemplary via holes 216a and 216b positioned over respective contact regions (not shown) of transistors 214a and 214b and a trench 216c connecting the via holes. The exemplary embodiment forms layer 216 from photoresist, through use of spincoating, lithography, and photoresist remover. Some embodiments use plasma ashing to pattern the photoresist. Also, in the exemplary embodiment, via holes 216a and 216b are cylindrical with diameters of about 1000 nanometers and depths of about 500 nanometers. Trench 216c is less than 0.50 microns wide and at least one micron deep. The invention, however, is not limited to any particular mask material, formation technique, geometry, or dimensions.

Figure 2 shows that the exemplary method next forms a conductive structure 218 on mask 216, with one or more portions of the conductive structure contacting one or more exposed portions of the transistors. In the exemplary embodiment, this entails depositing a 20-30-nanometer-thick copper-, silver-, or gold-based seed layer (not shown separately) using a chemical-vapor-deposition, ionized-magnetron sputtering technique, or DC magnetron self-sputtering technique, and then electroplating additional copper-, silver-, or gold-based material on the seed layer to a total thickness of, for example, 0.5 microns. (As used herein, a copper-, silver-, or gold-based material includes at least 25 weight-percent of the base material.) An exemplary chemical-vapor-deposition technique follows a procedure such as that described in Y. Senzaki, "Chemical Vapor Deposition of Copper Using a New Liquid Precursor with Improved Thermal Stability," MRS Conference Proceedings of Advanced Metallization and Interconnect Systems for ULSI Applications in 1997, ULSI XIII, P. 451-455, 1998, which is incorporated herein by reference. This

procedure yields copper films at a typical deposition rate of 150-170 nanometers per minute at wafer temperatures of 195-225°C. The resistance of these films is in the range of 2.0 micro-ohm-centimeter after annealing at 400°C for five minutes.

Exemplary ionized sputtering technique and d-c magnetron sputtering techniques follow procedures similar to those outlined in S. M. Rossnagel et al., Metal Ion Deposition from Ionized Magnetron Sputtering Discharge," J. Vac. Sci. Technology B, 12(1), p. 449-453, 1994. And Z. J. Radzimski et al, "Directional Copper Deposition using D-C Magnetron Self-sputtering," J. Vac. Sci Technology B 16(3), p. 1102-1106, 1998. Exemplary conditions for the ionized-magnetron sputtering operation are: target power range of 10-30 kilowatts for a 200-300 millimeter diameter wafer (or integrated-circuit assembly), RF coil power at 3-5 kilowatts, negative DC bias of 100-200 volts, sputtering argon gas pressurized at 1-35 millitorrs. Ionized-magnetron sputtering, which provides greater acceleration of the metal deposition material than conventional sputtering, forces the sputtered material to more closely conform to the interior profiles of holes and trenches of the targeted surface.

Notably, the exemplary embodiment omits formation of an adhesion layer to promote adhesion of copper (or other materials) to the mask layer. Some embodiments use a 20-50 nanometer-thick layer of titanium nitride (TiN) over the transistor contacts as an adhesion layer and a diffusion barrier. However, other embodiments provide an adhesion layer of titanium nitride. After depositing the conductive material, the exemplary method removes excess material, for example, using a chemical-mechanical planarization or polishing procedure.

Next, as Figure 3 shows, the exemplary method forms a mask layer 220 over conductive structure 218. Mask layer 220 includes an opening (via) 220a which exposes a portion of conductive structure 218 and a trench 220b which intersects opening 220a. Exemplary formation of conductive structure follows a procedure similar to that used to form mask layer 216 and occurs with at least a portion of mask layer 216 still in place.

Figure 4 shows that the exemplary method next forms a conductive structure 222 on mask 216, with portions of structure 222 contacting exposed portions of conductive structure 218. In the exemplary embodiment, this entails depositing a 20-30-nanometer-thick copper-, silver-, or gold-based seed layer and electroplating additional copper-, silver-, or gold-based material to an exemplary thickness of 0.5 microns. Excess material is then removed using a chemical-mechanical planarization or polishing procedure. Subsequently, one or more higher-level conductive structures can be formed similarly.

Figure 5 shows that after forming conductive structure 222, the method removes at least a portion of mask structures 216 and 220, defining one or more spaces or voids 224 around conductive structures 218 and 222. Without the surrounding masks, conductive structures 218 and 222 appears as a two-level airbridge. The exemplary embodiment removes substantially all of the mask structures by ashing them in an oxygen plasma.

After removal of the mask structures, the exemplary method forms a diffusion barrier 226 on at least portions of conductive structures 218 and 222. In the exemplary embodiment, this entails growing or depositing a two-to-six nanometer-thick layer of WSiN over substantially all of conductive structures 218 and 222. Exemplary formation of this layer of WSiN occurs within a hybrid reaction chamber such as that described in co-filed and co-assigned patent application entitled Methods and Apparatus for Making Copper Wiring in Integrated Circuits. This application, attorney docket 303.618US1 (99-0469), is incorporated herein by reference.

More particularly, exemplary formation of diffusion barrier 226 entails forming a graded composition of tungsten silicide (WSi_x), with x varying from 2.0 to 2.5. This entails heating the assembly to a temperature of 360°C and introducing hydrogen, tungsten hexafluoride, and silane gases into a process chamber enclosing the assembly. The exemplary embodiment introduces the hydrogen and tungsten hexaflouride gases about one-to-three seconds before introducing the silane gas and stops introducing the silane gas about one-to-three seconds before stopping

introduction of the hydrogen and tungsten hexaflouride. Exemplary flow rates for the silane and tungsten hexaflouride gases are respectively 1000 sccm and 14 sccm. These flow rates result in a composition of $WSi_{2.3}$, with a growth rate of approximately 50 nanometers per minute.

To complete the diffusion barrier, the exemplary method nitrides the graded composition of WSi_x, forming WSi_xN_y. The exemplary nitridation follows an electron-cyclotron-resonance (ECR) plasma nitridation procedure. One version of this procedure is described in A. Hirata et al., WSiN Diffusion Barrier Formed by ECR Plasma Nitridation for Copper Damascene Interconnection, Extended Abstracts of 1998 International Conference on Solid State Devices and Materials, p. 260-261, which is incorporated herein by reference. This entails introducing nitrogen gas and argon gas into the chamber, with the argon gas exciting a plasma. In the exemplary embodiment, the WSi_xN_y is not a compound-forming barrier, but a stuffed barrier, which prevents diffusion by stuffing nitrogen atoms into diffusion paths, such as interstitial sites, within the tungsten silicide. Other embodiments uses diffusion barriers having different compositions and thicknesses, and some entirely omit a diffusion barrier.

Figure 7 shows that after completion of diffusion barrier 226, the exemplary method fills at least a portion of the remainder of space 224 (denoted 224' in Figure 6) with one or more insulative materials. The exemplary embodiment fills substantially all of space 224, which was previously occupied by mask structures 216 and 220, with a single dielectric material using a single procedure. More particularly, the exemplary embodiment vapor deposits a silicon oxide, such as SiO_2, or low-k (that is, low-dielectric-constant) materials, such as xerogels or aerogels. Various methods, such as physical-vapor deposition, chemical-vapor deposition, spin-coating, sol-gel procedures, and so forth can be used to apply these dielectrics.

Figure 8 shows one example of the unlimited number of applications for one or more embodiments of the present invention: a generic integrated memory circuit 600. Circuit 600, which operates according to well-known and understood

principles, is generally coupled to a processor (not shown) to form a computer system. More precisely, circuit 600 includes a memory array 642 which comprises a number of memory cells 643a-643d, a column address decoder 644, and a row address decoder 645, bit lines 646, word lines 647, and voltage-sense-amplifier circuit 648 coupled to bit lines 646.

In the exemplary embodiment, each of the memory cells, the address decoders, and the amplifier circuit includes one or more copper-, silver, or gold-based conductors according to the present invention. Other embodiments, use conductors of other materials, made in accord with one or more methods of the present invention. In addition, connections between the address decoders, the memory array, the amplifier circuit are implemented using similar interconnects.

Conclusion

In furtherance of the art, the inventors have one or more exemplary methods for making integrated-circuit wiring from materials, such as copper-, silver-, and gold-based metals, some of which allow fabrication of wiring with fewer steps and lower electrical resistance than some conventional methods. One exemplary method initially forms a first mask and a first metal structure on the first mask and then forms a second mask and a second metal structure on the second mask, with the first mask and first metal structure still in place. Continuing, this exemplary method removes both masks in a single removal procedure, forms a diffusion barrier to both metal structures in a single formation procedure, and fills insulative material in and around both metal structures in a single fill procedure. Applying one or more procedures across multiple wiring levels, as in this embodiment, ultimately precludes the necessity of applying these procedures separately to each wiring level and thus promises to simplify fabrication.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which embraces all ways of

practicing or implementing the invention, is defined only by the following claims and their equivalents.